**Computer Architecture**

**Paper Structure**

**Question 1 :**

* **Basic Logic Gates and Circuits**
* **SOP & POS Expressions**
* **Boolean Algebra Simplification using K Maps**
* **Basic Electronics**

**Question 2 :**

* **Computer Organization**
* **The hardware composition**
* **Memory management**
* **Fetch Execution cycle**
* **Busses terminology**

**Question 3 :**

* **Instruction Addressing**
* **Combinational Circuits**

**Question 4 :**

* **Sequential circuits - 15**
* **Pipelining - 10**

**In a pipelined processor an instruction is executed through four stages as follows, and the times taken to each stage is mentioned as follows. Find the minimum time required to complete four instructions which are exactly similar.**

|  |  |
| --- | --- |
| **Fetch** | **4** |
| **Decode** | **8** |
| **Execute** | **12** |
| **Store** | **4** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **4** | **8** | **12** | **16** | **20** | **24** | **28** | **32** | **36** | **40** | **44** | **48** | **52** | **56** | **60** | **64** |  |  |  |
| **I1** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **I2** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **I3** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| **I4** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**Calculate the total pipeline delay?**

|  |  |
| --- | --- |
| **Instruction** | **Delay** |
| **I1** | **0** |
| **I2** | **12** |
| **I3** | **24** |
| **I4** | **36** |
| **Total** | **72** |

**Summary**

**Structural Hazzard – Trying to use same resource by multiple instructions at the same time.**

**Solutions – Use an empty cycle (stall) to delay**

**Acquire more resources to do the job**